AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1.   (Currently Amended)   A register file for a data processing system comprising:

a an unbanked memory unit having a plurality of memory locations, each memory location being addressable by an encoded address, wherein the encoded address corresponds to at least one register and processor mode; .

input ports to receive inputs for addressing at least one of the memory locations using an encoded address; and

output ports to output data from at least one of the memory locations addressable by an encoded address.

2.   (Currently Amended)   The register file of claim 1, wherein a plurality of registers correspond to the plurality of memory locations of the unbanked memory unit.

3.   (Original)   The register file of claim 2, wherein each register is addressable by a corresponding encoded address.

4.   (Original)   The register file of claim 3, wherein at least two registers are capable of being accessed in different processor modes using the same encoded address.

5.   (Currently Amended) The register file of claim 1, wherein the plurality of memory locations are discontinuous in the unbanked memory unit.

6.   (Original) The register file of claim 1, wherein a bit width of the plurality of memory locations is scalable to any arbitrary bit width size.

7.   (Original) The register file of claim 2, wherein inputs are received associated with at least one register and processor mode, and wherein at least one of the outputs is data from a register associated with an encoded address obtained from the received inputs.

8.   (Currently Amended) The register file of claim 7, wherein data is outputted from the unbanked memory unit for at least two instructions.

9.   (Original) The register file of claim 2, wherein inputs are associated with at least one register and processor mode, and wherein one of the inputs is data to be written in a register associated with an encoded address obtained from the received inputs.

10.   (Original) The register file of claim 9, wherein data for at least two retired instructions is to be written in at least two registers.

11. (Original) The register file of claim 1, further comprising:

an address encoder for each input port, the address encoder to provide an encoded address for accessing one of the memory locations.

12. (Original) The register file of claim 11, further comprising:

a latch to latch an encoded address from the address encoder; and

a selector coupled to the latch and the address encoder, the selector to select the encoded address from either the latch or the address encoder.

13. (Original) The register file of claim 10, wherein the latch stores the encoded address as a pipeline storage of the encoded address.

14. (Currently Amended) A register file for a data processing system comprising:

unbanked memory means having a plurality of memory locations, each memory location being addressable by an encoded address, wherein the encoded address corresponds to at least one register means and processor mode;

input means to receive inputs for addressing at least one of the memory locations using an encoded address; and

output means to output data from at least one of the memory locations addressable by an encoded address.

15.   (Currently Amended) The register file of claim 14, wherein a plurality of register means correspond to the plurality of memory locations of the unbanked memory means.

16.   (Original) The register file of claim 15, wherein each register means is addressable by a corresponding encoded address.

17.   (Original) The register file of claim 16, wherein at least two register means are capable of being accessed in different processor modes using the same encoded address.

18.   (Currently Amended) The register file of claim 14, wherein the plurality of memory locations are discontinuous in the unbanked memory means.

19.   (Original) The register file of claim 14, wherein a bit width of the plurality of memory locations is scalable to any arbitrary bit width size.

20.   (Original) The register file of claim 16, wherein inputs are received associated with at least one register means and processor mode, and wherein at least one of the outputs is data from a register means associated with an encoded address obtained from the received inputs.

21. (Currently Amended) The register file of claim 20, wherein data is outputted from the <u>unbanked</u> memory means for at least two instructions.

22. (Original) The register file of claim 15, wherein inputs are associated with at least one register means and processor mode, and wherein one of the inputs is data to be written in a register means associated with an encoded address obtained from the received inputs.

23. (Original) The register file of claim 22, wherein data for at least two retired instructions is to be written in at least two register means.

24. (Original) The register file of claim 14, further comprising:

addressing means for each input port, the addressing means to provide an encoded address for accessing one of the memory locations.

25. (Original) The register file of claim 24, further comprising:

latching means to latch an encoded address from the address encoder; and

selecting means coupled to the latching means and the addressing means, the selecting means to select the encoded address from either the latching means or the addressing means.

26. (Original) The register file of claim 23, wherein the latching means stores the encoded address as a pipeline storage of the encoded address.

27-50. (Cancelled)

51.   (Currently Amended) A processor comprising:

an integrated circuit including

a ~~an~~ <u>unbanked</u> memory unit having a plurality of memory locations, each memory location being addressable by an encoded address, wherein the encoded address corresponds to at least one register and processor mode; and

at least one address encoder to provide at least one encoded address for addressing at least one of the memory locations.

52.   (Currently Amended) The processor of claim 51, wherein a plurality of registers correspond to the plurality of memory locations in the <u>unbanked</u> memory unit.

53.   (Original)   The processor of claim 52, wherein each register is addressable by a corresponding encoded address.

54.   (Original) The processor of claim 53, wherein at least two registers are capable of being accessed in different processor modes using the same encoded address.

55.   (Currently Amended) The processor of claim 51, wherein the plurality of memory locations are discontinuous in the <u>unbanked</u> memory unit.

56. (Original) The processor of claim 51, wherein a bit width of the plurality of memory locations is scalable to any arbitrary bit width size.

57. (Original) The processor of claim 51, wherein each address encoder includes input ports to receive inputs associated with at least one register and processor mode in providing a corresponding encoded address.

58. (Original) The processor of claim 57, wherein each address encoder includes logic circuitry to obtain the corresponding encoded address based on the received inputs.

59. (Original) The processor of claim 58, wherein the logic circuitry includes at least one of a programmable gate array (PGA) or a field programmable gate array (FPGA).

60. (Original) The processor of claim 51, wherein the processor is at least one of an embedded processor and a microprocessor.

61. (Original) A data processing system comprising a memory mapped register file for accessing a plurality of memory locations, each memory location being addressable by an encoded address, wherein the encoded address corresponds to at least one register and processor mode.

62.   (Original) The data processing system of claim 61, wherein a plurality of registers correspond to the plurality of memory locations.

63.   (Original) The data processing system of claim 62, wherein each register is addressable by a corresponding encoded address.

64.   (Currently Amended) A processor comprising:

circuit means including:

unbanked memory means having a plurality of memory locations, each memory location being addressable by an encoded address, wherein the encoded address corresponds to at least one register means and processor mode; and

at least one addressing means to provide at least one encoded address for addressing at least one of the memory locations.

65.   (Currently Amended) The processor of claim 64, wherein a plurality of register means correspond to the plurality of memory locations of the unbanked memory unit means.

66.   (Original) The processor of claim 65, wherein each register means is addressable by a corresponding encoded address.

67.   (Original) The processor of claim 66, wherein at least two register means are capable of being accessed in different processor modes using the same encoded address.

68.   (Currently Amended) The processor of claim 64, wherein the plurality of memory locations are discontinuous in the unbanked memory means.

69.   (Original) The processor of claim 64, wherein a bit width of the plurality of memory locations is scalable to any arbitrary bit width size.

70.   (Original) The processor of claim 64, wherein each addressing means includes input means to receive inputs associated with at least one register means and processor mode in providing a corresponding encoded address.

71.   (Original) The processor of claim 70, wherein each addressing means includes logic means to obtain the corresponding encoded address based on the received inputs.

72.   (Original) The processor of claim 71, wherein the logic means includes at least one of a programmable gate array (PGA) or a field programmable gate array (FPGA).

73.   (Original) The processor of claim 64, wherein the processor is at least one of an embedded processor and a microprocessor.

74.   (Currently Amended) An integrated circuit method comprising:

configuring the integrated circuit to receive inputs;

configuring the integrated circuit to determine an <u>unbanked</u> encoded address based on the received inputs, wherein the <u>unbanked</u> encoded address corresponds to at least one register and processor mode; <u>and</u>

configuring the integrated circuit to access a register using an <u>unbanked</u> encoded address; and configuring the integrated circuit to output data from the accessed register.

75.   (Original) The method of claim 74, further comprising:

configuring the integrated circuit to output data for multiple instructions.

76.   (Original) The method of claim 74, further comprising:

configuring the integrated circuit to write data to the accessed register.

77.   (Original) The method of claim 76, further comprising:

configuring the integrated circuit to write data to one or more accessed registers for multiple executed instructions.

78.   (Currently Amended) A method for accessing ~~a~~ an unbanked memory unit having a plurality of memory locations comprising:

receiving a memory request for accessing the unbanked memory unit, the memory request including a register index input and a processor mode input;

encoding the register index input and processor mode input to obtain an encoded address;

accessing at least one of the memory locations of the unbanked memory unit in accordance with the encoded address, wherein the encoded address corresponds to at least one register and processor mode; and

writing data into or reading data from the accessed memory location.

79.   (Original) The method of claim 78, wherein writing data into or reading data from the accessed memory location includes writing data into or reading data from the accessed memory location for multiple instructions.

80.   (Currently Amended) ~~A~~ An unbanked memory unit comprising:

a plurality of memory locations addressable by encoded addresses, wherein each encoded address corresponds to at least one register and processor mode.

81.   (Currently Amended) The unbanked memory unit of claim 80, wherein a plurality of registers correspond to the plurality of memory locations.

82.   (Currently Amended)   The <u>unbanked</u> memory unit of claim 81, wherein each register is associated with an index that maps to a corresponding encoded address based on at least one processor mode.

83.   (Currently Amended)   The <u>unbanked</u> memory unit of claim 82, wherein each encoded address is capable of mapping to one or more indices associated with a register and a particular processing mode.

84.   (Currently Amended)   The <u>unbanked</u> memory unit of claim 80, wherein the plurality of memory locations of the <u>unbanked</u> memory unit addressable by an encoded address are discontinuous.

85.   (Currently Amended)   The <u>unbanked</u> memory unit of claim 80, wherein a bit width of the plurality of memory locations is scalable to any arbitrary bit width size.